Development of Accurate Techniques for Design of Trans Impedance Amplifiers

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ABSTRACT

Transimpedance Amplifier (TIA) plays a significant role in today's high speed fiber net communication. TIA is the first block in an optical transceiver utilising Visible region of electromagnetic spectrum. For high speed fiber net links, the parasitic capacitance encountered during design and manufacture restrict the bandwidth of operation. This report provides an insight on how to design a high bandwidth TIA for fiber optic communication. The project is focused on designing a high bandwidth, low power TIA. The high bandwidth TIA is designed on the principle of inductive peaking. The entire design of the TIA, was done in Cadence Virtuoso. The process technology is 45 nanometers. The simulation was performed in Analog Design Environment. The simulated results showed improvements compared to the expected results.

***Keywords*:** High bandwidth, High gain, low power, low noise**.**

1. INTRODUCTION

An amplifier is a device which increases the strength of the input weak signal. Based on the input electrical signal there are 4 types of amplifiers.

1. Voltage amplifier (input voltage, output voltage).
2. Current amplifier (input current, output current).
3. Trans conductance amplifier (input voltage, output current).
4. Trans impedance amplifier (input current, output voltage).

Trans Impedance Amplifier (TIA) is the first block of optical receivers utilizing Visible region of the electromagnetic spectrum. The input to TIA is mostly from photo diodes and the current values are in micro amperes to picoamperes. Hence design of a formidable TIA for a specific application is quite challenging. Optical receivers are used in simple infrared receivers, high speed fiber optic communication and light-based instrumentation. Optical receivers convert photons to current via photo diode and the trans impedance amplifier converts the current into voltage. High speed digital communication requires high throughput with enough sensitivity to keep bit error rate low. The signals are in the range of nano amperes to pico amperes. Hence to realise the minimum requirements of ADC input voltages, sufficient trans impedance gain is required.

2. FUNDAMENTALS OF TIA

The Figure 1, represents an inverting amplifier. Assuming ideal conditions, due to infinite input impedance the input current is forced to flow through the feedback resistance.

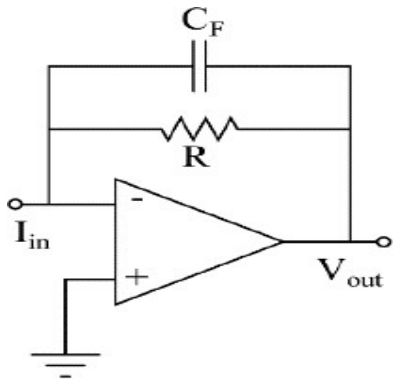

Figure 1. Inverting amplifier as TIA [19]

The output voltage is just the product of input current and feedback resistance, with a change in phase. The overall trans impedance gain is determined by the feedback resistance 'R'. Now, if Giga ohm trans impedance gain is required, then the feedback resistance should also be Giga ohms. In IC design philosophy, Giga ohm resistance consumes enormous area as well as power. Considering all non-idealities of OpAmp, virtual ground can be achieved with high gain. Unlike ideal OpAmp} with infinite bandwidth, the non-ideal Opamp bandwidth of operation is restricted to its UGB (Unity Gain Bandwidth). Typically, the UGB of OpAmp does not exceed 2GHz with sufficiently high gain to achieve virtual ground as well. Hence cannot be used for Gbps (Giga bits per second) fiber optic communication. Due to finite input impedance, output impedance, DC voltage and current offset, the output voltage is no longer just a simple product of input current and feedback resistance. It depends on the transfer function of inverting amplifier as well as load.

BANDWIDTH EXTENSION TECHNIQUES

The photo diode capacitance influences the transfer function of the TIA, thereby playing a significant role in determining the bandwidth of the TIA. Bandwidth extension techniques are used to compensate for the loss in bandwidth generated by the pole of the photo diode capacitance.

INDUCTIVE PEAKING

The idea of inductive peaking is to use an inductor to resonate with the parasitic capacitive load which usually limits the bandwidth, thereby increasing speed and bandwidth without significant power consumption or loss of gain. This can be done by placing the inductor in shunt or in series. Here series peaking is employed. On-chip spiral inductors are used in spite of their large area consumption. The mathematical analysis of inductive peaking reveals that the peaking can be achieved by either Pole-Zero cancellation or Complex Conjugate Pole Compensation.

POLE-ZERO CANCELLATION

This technique is used when the photo diode capacitance is of a significant value such that it produces real poles from the transfer function. The addition of an inductor cancels the effects of the dominant pole upon reaching resonance.

COMPLEX CONJUGATE POLE COMPENSATION

This technique is used when the photo diode capacitance is a value such that it produces complex conjugate poles. Hence addition of an inductor will change the damping factor as well as the natural frequency of operation of the complex conjugate poles.

INVERTER BASED TIA WITH RESISTIVE FEEDBACK

The inverter-based TIA is a simple inverter circuit with RL feedback for enhancing the bandwidth as shown in Figure 2.

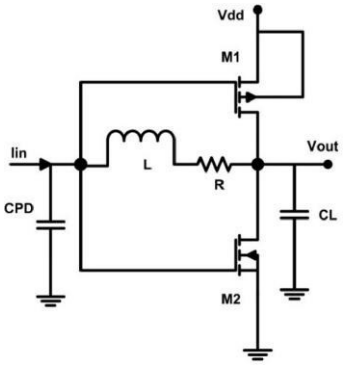

Figure 2. Inverter based TIA with resistive feedback [17]

The input current is made to flow through the feedback network. The feedback impedance determines the overall trans impedance gain, while the inductive feedback provides cancellation of dominant pole or complex conjugate pole from the photo diode. This circuit is typically used in high bandwidth optical communication applications.

The small signal model of the inverter TIA is as shown in Figure 3 below.

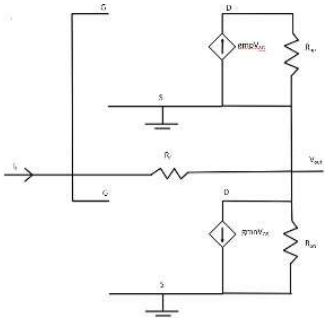

Figure 3. Small signal model of inverter-based TIA with resistive feedback

Solving the small signal model for trans impedance reveals that, the overall trans impedance Z_T is given by below equation.

$$Z_T = \left(1 - \frac{\square\square}{\square}\right)(R \,||\, R') \qquad (1.1)$$

Where, R = 1/G, G is the sum of trans conductance of both the MOSFETs.

R', is the parallel combination of Channel Length Modulation (CLM) resistance of the MOSFETs.

R_F is the feedback resistance.

3. DESIGN METHODOLOGY

The section discusses the various techniques which can be utilized to design efficient high performance TIAs.

COMMON GATE TIA FOR HIGH GAIN

1. The Common gate TIA full transistor design consists of three transistors.
2. The output is across the output of the drain resistance of the middle transistor.
3. The PMOS provides the required DC current and the finite resistance can be influenced by the CLM.
4. Beginning with PMOS, the three terminals are determined as follows. The source is connected to power supply line

7. Based on the required resistance, the corresponding drain voltage is obtained.
8. The MOSFET is ensured to be in saturation condition. This allows to calculate the ratio of gm and Id from the DC parameters of PMOS.
9. Having calculated the Gm/Id ratio, the remaining MOSFETs are subjected to calculations of DC operating points by Gm/Id methodology.
10. The drain voltage is known for second MOSFET, but gate as well as source voltage needs to be calculated. The source voltage is fixed such that it is able to turn on the N-channel MOSFET (NMOS) below it.
11. Now the source voltage is known. The MOSFETs are subjected to DC analysis, where a plot of Gm/Id vs VGS is obtained.
12. The calculated Gm/Id from PMOS will determine the gate voltage. This is calculated having fixed the width.
13. A parametric analysis of Gm/Id vs VGS, with varying width can provide the required gate voltage based on the design constraints.
14. The foot NMOS aspect ratio is determined by performing DC analysis where a plot is Gm/Id vs width is obtained. The corresponding width for the calculated Gm/Id is obtained.

DIFFERENTIAL COMMON GATE TIA FOR HIGH BANDWIDTH

1. The CG stage is designed using the methodology discussed in the above section.
2. The differential signalling is obtained by utilising a CS stage such the amplitudesof both the stages remain the same. The equations are present in the design equations section.
3. The resistor value is typically fixed.
4. The width of the NMOS is varied to obtain the required trans conductance. Typically, the resistance is chosen to be same as that of the CG stage. This resistance can be either a little low or high from that of the CG stage.
5. Once the required trans conductance is obtained, the differential signalling is obtained with small error in the amplitudes.
6. The error can be minimized by using a high precision resistor.

REGULATED GATE CASCODE (RGC) FOR HIGH GAIN

1. The Regulated Gate Cascode TIA full transistor design consists of five transistors.
2. The output is across the output of the drain resistance of the middle transistor.
3. The PMOS provides the required DC current and the finite resistance can be influenced by the CLM.
4. Beginning with PMOS, the three terminal voltages are determined as follows. The source is connected to power supply line.
5. The gate voltage is fixed such that the MOSFET is in saturation.
6. The MOSFET is swift with a DC analysis to plot resistance due to vs drain voltage.
7. Based on the required resistance, the corresponding drain voltage is obtained.
8. The MOSFET is ensured to be in saturation condition. This allows to calculate the ratio of gm and Id from the DC parameters of PMOS.
9. Having calculated the Gm/Id ratio, the remaining MOSFETs are subjected to calculations of DC operating points by Gm/Id methodology.
10. The drain voltage is known for second MOSFET, but gate as well as source voltage needs to be calculated. The source voltage is fixed such that it is able to turn on the NMOS below it.
11. Now the source voltage is known. The MOSFETs are subjected to DC analysis, where a plot of Gm/Id vs VGS is obtained.
12. The calculated Gm/Id from PMOS will determine the gate voltage. This is calculated having fixed the width.
13. A parametric analysis of Gm/Id vs VGS, with varying width can provide the required gate voltage based on the design constraints.
14. The foot NMOS aspect ratio is determined by performing DC analysis where a plot is Gm/Id vs width is obtained. The corresponding width for the calculated Gm/Id is obtained.
15. The CS amplifier is designed using the GM/Id methodology using the ratio calculated from PMOS.
16. The reference design for Gm/Id methodology DC operating conditions are already available from the CG stage.

INVERTER BASED TIA FOR HIGH BANDWIDTH

1. The theory of the inverter-based TIA was discussed in fundamentals of TIA. There are two impedances to be considered from the trans impedance expression. The feedback resistance and the inverter resistance due to CLM.
2. The gain for high bandwidth is typically less than 1k.
3. The inverter resistance is designed first and then a suitable feedback resistance is plugged.
4. The inverter resistance can be designed twice the required gain value which provides an out of phase response.
5. The inverter resistance can be designed half the required gain value which provides in-phase response.
6. The channel length is fixed to the desired value or as per given specification or available technology.
7. The inverter is first provided with a short circuit network.
8. AC analysis is performed and a plot of gain vs frequency is obtained.
9. The obtained plot is now subjected to a parametric analysis with varying width.
10. The overall parametric plot helps in determining the required inverter short circuit impedance.
11. The short circuit is now replaced with a feedback resistance according to the equation (1.1).
12. The series peaking and inductive peaking can be utilised to achieve the required 3dB bandwidth.
13. Two inductors are added in the circuit. The series peaking is introduced by adding an inductor in series with the source. The inductive peaking is achieved by adding an inductor in the feedback.
14. A parametric analysis of the AC response is performed to choose the minimum value of inductors which provide the minimum bandwidth required.

SHUNT FEEDBACK TIA FOR HIGH BANDWIDTH

1. The theory of the inverter-based TIA was discussed in fundamentals of TIA section. There are two impedances to be considered from the trans impedance expression. The feedback resistance and the inverter resistance due to CLM.
2. The NMOS resistance is designed first and then a suitable feedback resistance is plugged if required.
3. The feedback resistance should be the dominant resistance which determines the overall trans impedance.
4. The channel length is fixed to the desired value or as per given specification or available technology.
5. The NMOS is first provided with a short circuit network.
6. AC analysis is performed and a plot of gain vs frequency is obtained.
7. The obtained plot is now subjected to a parametric analysis with varying width.
8. The overall parametric plot helps in determining the required NMOS short circuit impedance.
9. The short circuit can be replaced with a feedback resistance according to the equation (1.1). The series peaking and inductive peaking can be utilised to achieve the required 3dB bandwidth.

4. IMPLEMENTATION

The Figure 4, represents the implemented design of the Common Gate TIA for high gain applications. The aspect ratios are given in Table 1. The test bench source is modelled as an AC current source with capacitor of 200fF in parallel acting as the photo diode capacitance. The TIA is given a load capacitance of 100fF. The DC operating voltages at gate are 560mV, 1.54V and 850mV respectively from top to bottom of the circuit. An inductor is added to improve the 3dB bandwidth.

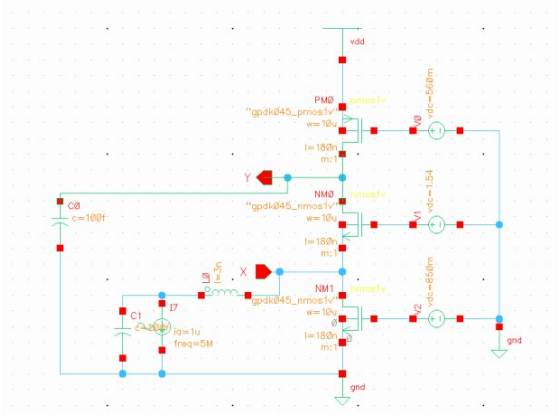

Figure 4. CG TIA for High Gain

Table 1. Transistor sizing of Common Gate TIA for High Gain

Transistor	Width (W)	Length (L)	Aspect ratio (W/L)
NM0	10µm	180nm	55.56
NM1	10µm	180nm	55.56
PM0	10µm	180nm	55.56

The Figure 5, represents the implemented design of the Common Gate TIA for high bandwidth applications. The aspect ratios are given in Table 2. The test bench source is modelled as a AC current source with capacitor of 200fF in parallel acting as the photo diode capacitance. The TIA is given a load capacitance of 100fF. The DC operating voltages at gate are 1.4V, 700mV for NMOS (NM0) and PMOS (NM1) respectively. The resistors 175Ω and 1.5kΩ are used to establish the DC operating point of the CG stage. The resistor 165Ω is used to bias the CS stage to obtain equal amplitude swings.

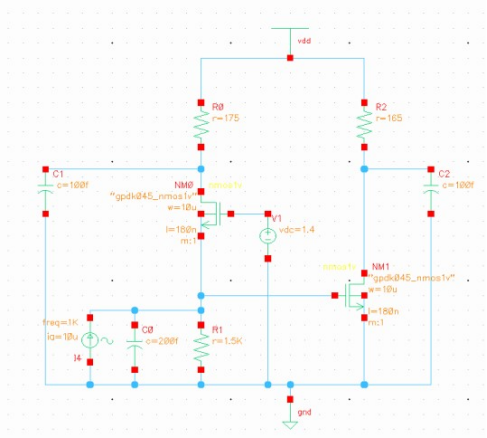

Figure 5. Differential Common Gate TIA for High Bandwidth

Table 2. Transistor sizing for Differential Common Gate TIA

Transistor	Width (W)	Length (L)	Aspect ratio (W/L)
NM0	10µm	180nm	55.56
NM1	10µm	180nm	55.56

The Figure 6, represents the implemented design of the RGC TIA for high gain applications. The aspect ratios are given in Table 3. The test bench source is modelled as an AC current source with capacitor of 200fF in parallel acting as the photo diode capacitance. The TIA is given a load capacitance of 100fF. The DC
operating voltages at gate are 1.1V, 1.1V and 743mV respectively for the PMOSs and CG NMOS (NM1) foot transistor.

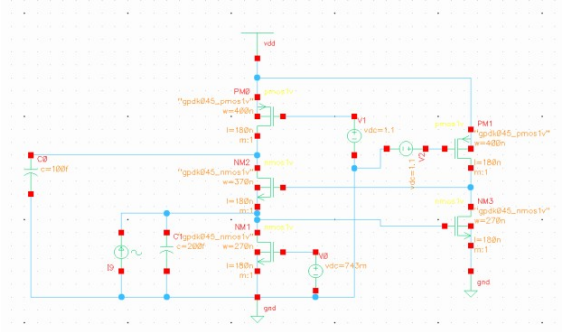

Figure 6. RGC TIA for High Gain

Table 3. Transistor sizing of RGC TIA for High Bandwidth

Transistor	Width (W)	Length (L)	Aspect ratio (W/L)
NM0	10µm	180nm	55.56
NM1	10µm	180nm	55.56
PM0	10µm	180nm	55.56
PM1	10µm	180nm	55.56

The Figure 7, represents the implemented design of the Inverter based TIA for high bandwidth applications. The aspect ratios are given in Table 4. The test bench source is modelled as an AC current source with capacitor of 200fF in parallel acting as the photo diode capacitance. The TIA is given a load capacitance of 100fF. The DC operating voltages at gate are 900V due to small resistive feedback. A feedback resistor of 100Ω is used to obtain the required gain. Two inductors of 2.2nH each are used to obtain series peaking as well as inductive peaking to enhance the bandwidth.

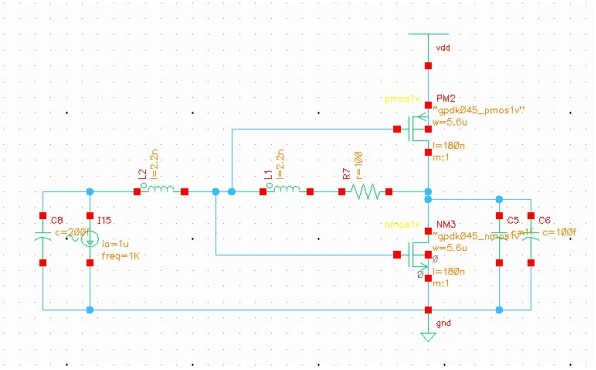

Figure 7. Inverter based TIA for High Bandwidth

Table 4. Transistor Sizing for Inverter Based TIA for High Bandwidth

Transistor	Width (W)	Length (L)	Aspect ratio (W/L)
NM0	5.6µm	180nm	31.11
NM1	5.6µm	180nm	31.11

The Figure 8 represents the implemented design of the Shunt Feedback TIA for high bandwidth applications. The aspect ratios are given in Table 5. The test bench source is modelled as an AC current source with capacitor of 200fF in parallel acting as the photo diode capacitance. The TIA is given a load capacitance of 100fF. The DC operating voltages at gate is determined by the resistive feedback. A feedback resistor of 300Ω is used to obtain the required gain from design equations calculations. The PMOS is grounded as it acting more of as a current source. Hence to achieve maximum current, the gate is grounded. Two inductors of 2.5nH each are used to obtain series peaking as well as inductive peaking to enhance the bandwidth.

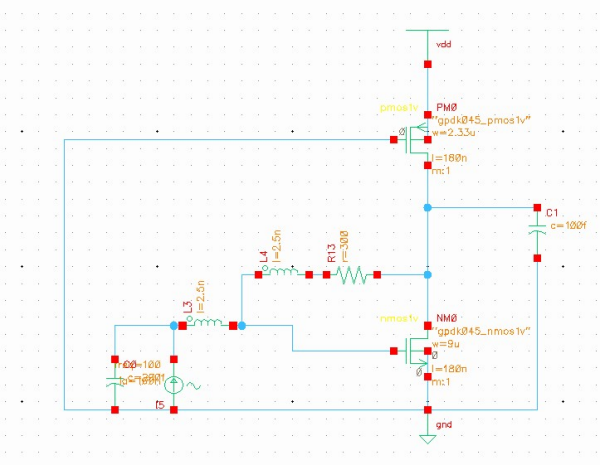

Figure 8. Shunt feedback TIA for High Bandwidth

Table 5. Transistor Sizing for Shunt Feedback TIA for High Bandwidth

Transistor	Width (W)	Length (L)	Aspect ratio (W/L)
NM0	9µm	180n	50
PM1	2.3µm	180n	12.78

5. RESULTS

The table below lists all the results of various analysis performed on the different implemented designs.

Table 6. Performance Comparison of implemented Circuits

Parameter	[1]	[2]	CG	Differential CG	RGC	Inverter TIA	Shunt Feedback TIA
Gain (dBΩ)	60	68.3	83.803	43.28	99.789	40.368	40.3801
Bandwidth (Hz)	1.64G	8.5G	80.97M	2.52G	15.99M	9.15G	3.5588G
Input noise (A/√Hz)	5.79p	11.6p	412.5p	682.2p	2.1n	168.5p	3.11n
Output noise (V/√Hz)	-	-	848.1p	584.7p	609.7p	923.9p	766.1p
Power (W)	760µ	81m	425.7µ	1.7m	68.78µ	5.54m	5.54m

The AC analysis is performed for a frequency range of 10Hz to 100GHz. The Noise analysis is swept for the same range of frequency. The power mentioned are an average value taken over a temperature range of 0°C to 100°C.

6. CONCLUSION

The Trans Impedance Amplifier is an important amplifier in today's fiber optic communication and now popular Near-Infra Red spectroscopy. This project focuses on developing TIA with very high bandwidth, very high trans impedance gain as well as methodologies to implement them. The fundamental TIA design using an OpAmp was discussed along with the major constraints imposed by that circuit. Later, alternate circuits with different topologies and approach specifically tailored for a particular application either bandwidth or gain was discussed. These designs have to be tuned to develop an optimized design with less trade-off. The TIA designs require a good methodology

with good accuracy and hence that would be the first objective. Selecting a particular topology for bandwidth, gain and implementing based on the developed methodology would be two objectives. The simulation was performed in Analog Design Environment. The simulated results showed improvements compared to the expected results. The Inverter based TIA had the lowest input referred noise with 168.5pA√Hz and 169.8p√Hz for high bandwidth and high gain respectively. The RGC topology was able to throttle very high gain with high accuracy and provided 99.789dBΩ and consumed the least power of 68.78µW. For the same gain design in high bandwidth, the shunt feedback TIA has more noise component. This arises for a fact that, the resistance of the topology is twice that of an inverter and the feedback resistance required to realize a given gain increases as well. The Differential CG TIA showed a significant improvement in noise performance over CG TIA with values 682.2pA√Hz and 4.562n√Hz respectively without much degradation in gain and power.

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